REMARKS

Claims 21, 22, 24, 25, and 28 have been amended. Claims 23 and 27 have been cancelled. No new matter has been introduced by the amendments.

The title of the invention has been amended as suggested by the Office Action.

Claims 21, 23, 24, 25, 27, 28, and 29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Zahorik et al., U.S. Patent No. 5,789,277 (Zahorik). Applicants respectfully traverse the rejection.

Amended independent claim 21 relates to a memory cell intermediate structure. As such, claim 21 recites "a memory cell intermediate structure comprising: a first conductor formed on said substrate; an insulator formed on said first conductor, at least one via formed within said insulator and extending to said first conductor; a metallic material formed in said at least one via; and a flowable oxide material localized only within said via and over said metallic material within said via."

Amended independent claim 25 recites "a programmable conductor random access memory intermediate structure, comprising: a metallic material formed on a surface of an insulating layer and within and over a bottom of a via in said insulating layer; and-a flowable oxide layer restricted within said via and over said metallic material within said via."

Zahorik discloses a chalcogenide memory cell having a lower conductive layer 120 of carbon, a layer 130 of chalcogenide material, and an upper conductive layer 140 of carbon. *See* col. 8, lines 25-30; *see also* Fig. 7. Zahorik also discloses a protective layer 150 of silicon dioxide over layers 120, 130, and 140. *See* col. 8, line 66 through col. 9, line 1; *see also* Fig. 7. Protective layer 150 is provided over the insulating layer 80 as

well. According to Zahorik, layer 150 protects layers 120, 130, and 140 within the pore 110 from attack by the chemical etchants used in subsequent operations. *See* col. 9, lines 5-7.

Zahorik fails, however, to teach or suggest a memory cell intermediate structure having, *inter alia*, "a flowable oxide material localized only within said via and over said metallic material within said via," as recited by claim 21. Zahorik similarly fails to teach or suggest a programmable conductor random access memory intermediate structure having, *inter alia*, "a flowable oxide layer restricted within said via and over said metallic material within said via," as recited by claim 25. For at least these reasons, Applicants respectfully submit that claim 21 and 25 are allowable over Zahorik.

Claims 23 and 27 have been cancelled. Claims 24, 28, and 29 depend from claims 21 and 25, and are allowable for at least the same reasons set forth above and on their own merits.

Claims 22, 26, and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Zahorik as applied to claims 21, 23-25, and 29 above, and further in view of Kozicki, U.S. Patent 6,487,106 and Iba, U.S. Patent No. 5,883,006. Applicants respectfully traverse the rejection.

Kozicki relates to a programmable microelectronic device and method of forming and programming same. Title. Kozicki discloses an electrode 130 over a substrate 110. *See* col. 6, line 51 through col. 7, line 4; *see also* FIG. 1. Kozicki also discloses a via in an insulating layer 150, and an ion conductor 140 and electrode 120 formed within the via. *See* FIG. 1. Kozicki fails, however, to teach or suggest a memory cell intermediate structure having, *inter alia*, "a flowable oxide material localized only

within said via and over said metallic material within said via," as recited by claim 21, from which claim 22 depends. Similarly, Kozicki fails to teach or suggest a programmable conductor random access memory intermediate structure having, *inter alia*, "a flowable oxide layer restricted within said via and over said metallic material within said via," as recited by claim 25, from which claim 26 depends. For at least these reasons, Applicants respectfully submit that claims 22 and 26 are allowable over the combination of Zahorik and Kozicki.

Iba relates to a method of making a semiconductor device using a flowable oxide film. Title. Specifically, Iba relates to a substrate 100 having a second insulating film 106 formed on a first insulating film 102. *See* col. 3, lines 50-51; *see also* FIG. 2(d) (reproduced below). The second insulating film 106 has a via formed therein.

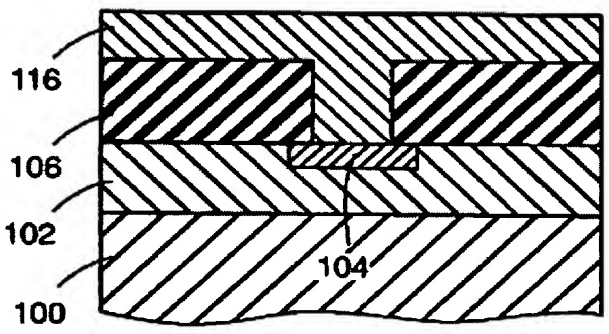

Fig. 2(d)

As illustrated by Iba's FIG. 2(d), the flowable oxide is provided on and over the surface of the second insulating film 106. Iba, therefore, fails to teach or suggest a memory cell intermediate structure having, *inter alia*, "a flowable oxide material localized only within said via and over said metallic material within said via," as recited by claim 21. Iba similarly fails to teach or suggest a programmable conductor random access memory intermediate structure having, *inter alia*, "a flowable oxide layer restricted within said via and over said metallic material within said via," as recited by

claim 25, from which claim 29 depends. Iba also fails to teach or suggest a programmable conductor random access memory intermediate structure having silicon oxide that "is in a flowable form in a temperature range of 50°C to 90°C," as recited by claim 29. For at least these reasons, Applicants respectfully submit that claim 29 is allowable over the combination of Zahorik and Iba

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: December 6, 2004

Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants